

WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device,
comprising:

5 a plurality of I/O slots arranged in parallel
along the peripheral portion of a chip within the inner
region of the chip and having input/output cells
connected thereto;

10 a plurality of pads arranged a predetermined
distance apart from each other above said I/O slot and
extending from the peripheral portion of the chip
toward the central portion;

15 a plurality of first wiring each having one end
positioned in said pad and having the other end
positioned in the peripheral region of the inner
portion of the chip above the I/O slot; and

a second wiring arranged in the outermost
peripheral region of the chip and serving to connect
the other end of each of the plural the first wiring to
a predetermined I/O slot.

20 2. The semiconductor integrated circuit device
according to claim 1, wherein said second wiring is
arranged between the first wiring and the first I/O
slot such that one end of the second wiring is
connected to the first wiring arranged in the second
25 I/O slot, with the other end being connected to the
first I/O slot.

3. A method of connecting the wiring of a

2095220-6078007

semiconductor integrated circuit device for connecting
a plurality of I/O slots arranged in parallel along the
peripheral portion of a chip within the inner region
of the chip and having input/output cells connected
5 thereto to a plurality of pads arranged a predetermined
distance apart from each other above said I/O slot
and extending from the peripheral portion of the chip
toward the central portion, comprising the steps of:

connecting each of said pads to the peripheral
10 portion above the I/O slot in the inner region of the
chip; and

connecting the peripheral portion in the inner
region of the chip to a desired I/O slot in the
outermost peripheral region of the chip.

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